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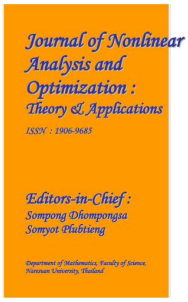


# HIGH CMRR VOLTAGE MODE INSTRUMENTATION AMPLIFIER USING A NEW CMOS SECOND-GENERATION CURRENT CONVEYOR REALIZATION

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**ABSTRACT:** The paper aims to design a high common-mode rejection ratio (CMRR) voltage mode instrumentation amplifier utilizing a novel CMOS second-generation current-controlled current conveyor (CCCII). The proposed amplifier architecture offers improved performance in terms of CMRR, which is crucial for accurately measuring signals in noisy environments. By leveraging the advantages of CMOS technology and the unique characteristics of the CCCII, the amplifier achieves enhanced linearity, stability, and noise performance compared to traditional designs. This work outlines the innovative approach to design instrumentation amplifier for applications requiring high precision and reliability in signal acquisition and measurement. Cadence Virtuoso tool with GPDK 45nm technology is used to test the performance of the design.

Keywords—CCCII, Current Feedback Operational Amplifier, instrumentation Amplifier, CMRR

## 1. INTRODUCTION

This manuscript is aimed at introducing an innovative methodology for designing a high CMRR voltage mode instrumentation amplifier. The impetus originates from the pressing need for precise measurements across diverse applications, spanning from medical devices to industrial sensors and communication systems. The conventional amplifier paradigms frequently grapple with the challenge of effectively mitigating unwanted common mode signals, consequently introducing inaccuracies in data acquisition. To confront this issue head-on and refine signal fidelity. The driving force behind this work lies in aspiration to redefine the boundaries of amplifier design, offering pragmatic solutions tailored to the exigencies of contemporary technology[1-8].

By harnessing the advantages conferred by the second-generation current-controlled conveyor, the objective is to design an amplifier capable not only of amplifying differential signals but also of mitigating common-mode interference to an unprecedented degree. We are acutely aware of the far-reaching implications that high CMRR instrumentation amplifiers can exert across various industries and applications. Whether it pertains to safeguarding the accuracy of medical diagnostics or optimizing the operational efficiency of industrial equipment, the reliability of signal amplification stands as a pivotal concern. Through the endeavors, to propel technological advancement by furnishing engineers and scientists with a potent instrument conducive to elevating the caliber and dependability of their measurements. This methodology unfolds through a meticulously structured exploration encompassing theoretical frameworks, design methodologies, simulation analyses, and empirical validations. Each phase of this odyssey is underpinned by an unwavering commitment to excellence and an indomitable resolve to surmount the inherent challenges ingrained within the realm of amplifier design. By meticulously documenting the procedural trajectory and elucidating the empirical findings, and endeavor to disseminate our insights and augment the collective reservoir of knowledge within the sphere of electronic instrumentation[9-17].

This work, thus, serves as an introductory overture to the overarching objectives underpinning our manuscript, affording a tantalizing glimpse into the innovative solutions and endeavor to forge. As delving deeper into subsequent sections, to extend an open invitation to readers to accompany on a voyage of discovery, wherein by unravel the intricacies of amplifier design and unearth the latent potential of the second-generation current-controlled conveyor realization. It is the collective aspiration to chart a course toward a new epoch characterized by heightened precision and unwavering reliability in the realm of signal processing[18-22].

## 2. SECOND GENRATION CURREENT CONVEYOR REALIZATION (CCCII)

The current conveyor serves as a fundamental building block, incorporating both negative and positive feedback mechanisms. It provides enhanced flexibility and can induce negative resistance. Meanwhile, the Current Controlled Conveyor (CCC) emerges as a dynamic structure alternative, offering versatility in CM applications. Notably, it features intrinsic resistance ($R_X$) between input ports X and Y, modulated by the bias current [17] & [22]. This inherent resistance stands as the primary distinction from CCII, eliminating the need for external resistance components. Consequently, circuit complexity is reduced, rendering CCCII particularly suitable for IC fabrication [18-20]. Fig.1 presents a block-level depiction of CCCII, showcasing its characteristic relationship and representing its matrix form in equation (1).

$$\begin{bmatrix} I_Y \\ V_X \\ I_{Z\pm} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & R_X & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix} \quad (1)$$

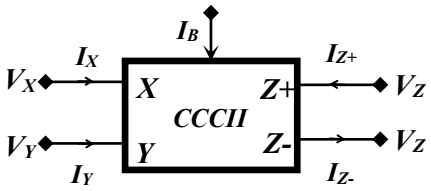


Figure 1. The structure of CCCII with input and output ports.

Dual output CCCII is basically a four-terminal device, that has two input ports X & Y, and an output port Z that delivers a current at the Z+ node and its replica at the Z- node. The device is illustrated with $I_Y = 0$, $V_X = V_Y + R_X * I_X$ and $I_Z = \pm I_X$. CCCII has an infinite input impedance at terminals Y and Z, whereas, the input port X has internal resistance $R_X$ that is tuned by the bias current $I_B$ is given as:

$$R_X = \frac{1}{g_{m2} + g_{m4}} \quad (2)$$

where $g_{mi}$ is the MOS transistor transconductance, assuming that both the transistors $M_2$ and $M_4$ are matched, $g_{m2}=g_{m4}$. This leads to:

$$R_X = \frac{1}{\sqrt{8\mu C_{OX}\left(\frac{W}{L}\right) I_B}} \quad (3)$$

The translinear loop consists of the transistors $M_1$- $M_4$ and is DC-biased with current mirrors $M_6$ & $M_7$ and $M_8$ & $M_9$. The input port current $I_X$ is replicated to $I_{Z+}$ and $I_{Z-}$ by the translinear loops. The current is also replicated using additional current mirrors $M_{10}$-$M_{13}$, $M_{14}$-$M_{16}$, and $M_{17}$-$M_{19}$ [24]. The aspect ratios of transistors of Fig. 2 are exhibited in Table I

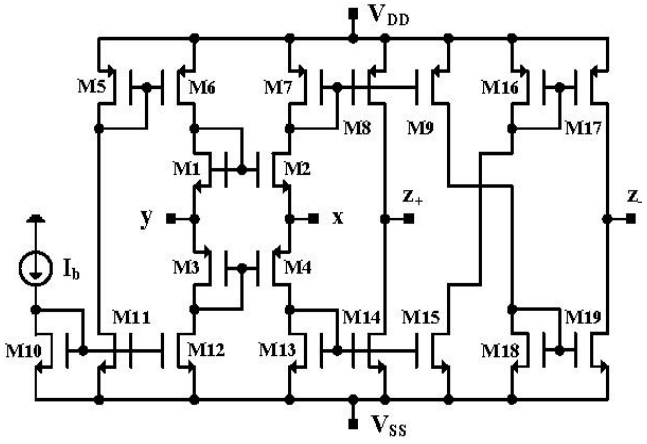


Figure 2. CCCII structure using MOS

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TABLE I. ASPECT RATIOS OF FIGURE 2. TRANSISTORS

| Transistor | Width (nm) | Length (nm) |
|---|---|---|
| $M_3$, $M_4$, $M_6$, $M_7$, $M_{12}$, $M_{13}$, $M_{14}$, $M_{18}$, $M_{19}$ | 120nm | 45nm |
| $M_1$, $M_2$, $M_5$, $M_8$, $M_9$, $M_{10}$, $M_{11}$, $M_{15}$, $M_{16}$, $M_{17}$ | 120nm | 35nm |

## 3. PROPOSED VOLTAGE MODE INSTRUMENTATION AMPLIFIER

The schematic diagram of the proposed voltage mode instrumentation amplifier circuit is presented in Figure 3. It is composed of one differential difference current conveyor circuit(DC) and two grounded resistances.The differential voltage expression is given as

$$V_{out} = G \cdot (V_2 - V_1) \quad (4)$$

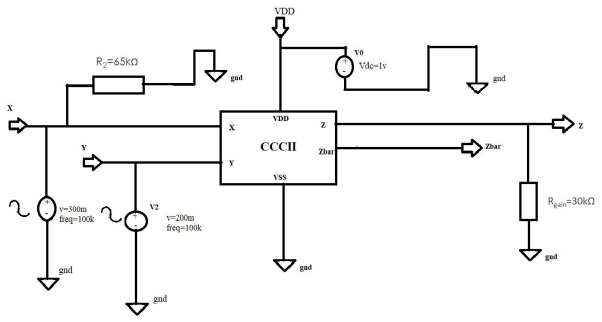

Figure 3. Proposed Instrumentation amplifier

Where $V_{out}$ is the output voltage. $V_2$ and $V_1$ are the input voltages, and G is the gain of the instrumentation amplifier.

$$V_o = (V_2 - V_1)(1 + \frac{2R_2}{R_{gain}})$$

$$A_v = (1 + \frac{2R_2}{R_{gain}})$$

## 4. SIMULATION RESULTS

Using Cadence virtuso tool, the topology shown in Figure. 3 is simulated. For this the supply voltage is fixed at ±1 V, the bias current $I_B$ is set at 50 $\mu A$, and the passive elements are chosen as $R_1$= 30 kΩ and $R_0$= 65 kΩ. The simulated output waveform of the topology has been shown in Figure 4, where the output voltage closely matches with theoretical anticipation carried out. The frequency of the produced signal can be varied by tuning the bias current. The frequency spectrum for the aforesaid values is also obtained (not shown here), which indicates the maximum frequency goes up to 100KHz. $I_B$ ranges from 10uA to 50uA by keeping the passive component values $R_1$=30 kΩ and $R_0$=65 kΩ. The variation of the output voltage with resistance is shown in Figure. 5. Likewise, the variation of gain concerning resistance is shown in Figure. 6 with the values $R_1$=30 kΩ, $R_0$=65kΩ, and bias current of 50 µA. The proposed amplifier gain is 9.03 and the delay is 125.7 ms.

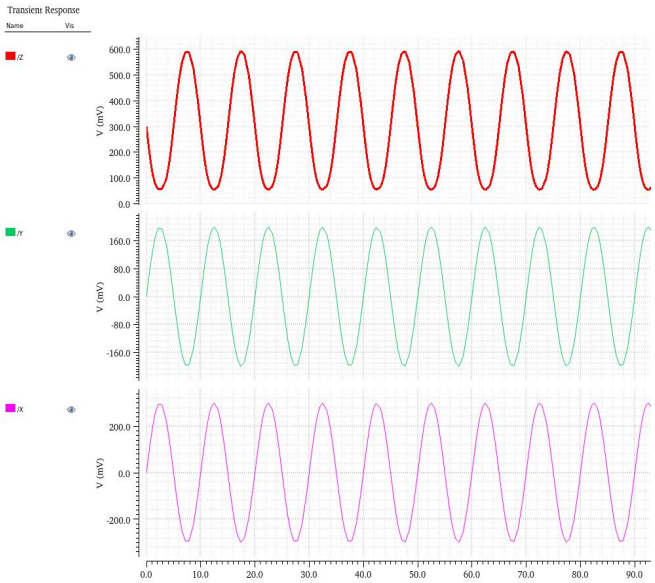


**Figure 4. Simulation results of the proposed topology**

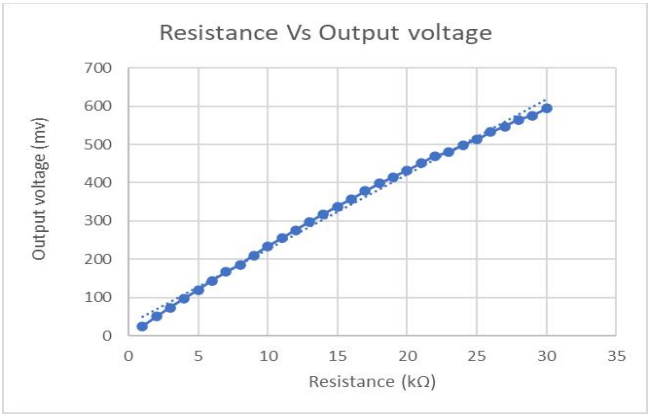


**Figure 5. Plot of output voltage concerning resistance**

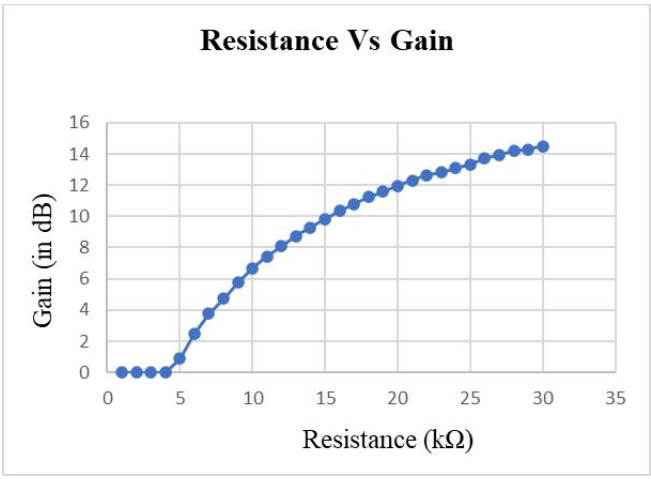


**Figure. 6 Plot of gain concerning resistance**

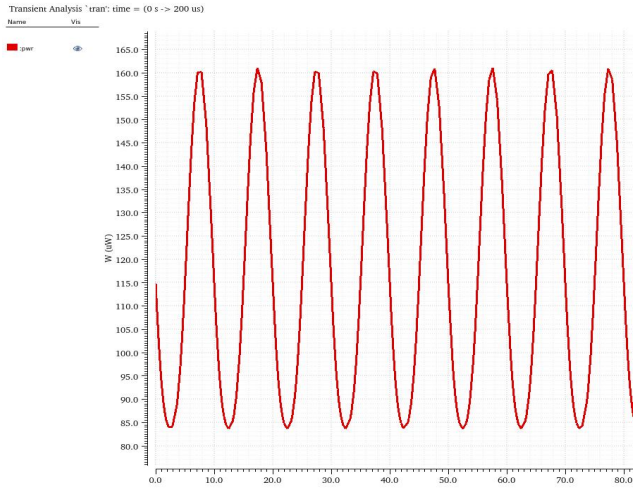


**Figure 7. Power response of proposed design**

The power dissipation for the proposed amplifier is 0.137 mW, which is quite less and useful for many signal processing applications.

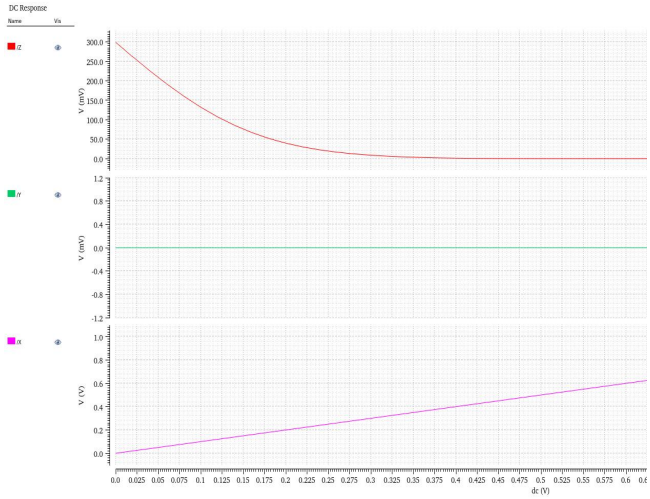

**Figure 8. DC response of the proposed topology**

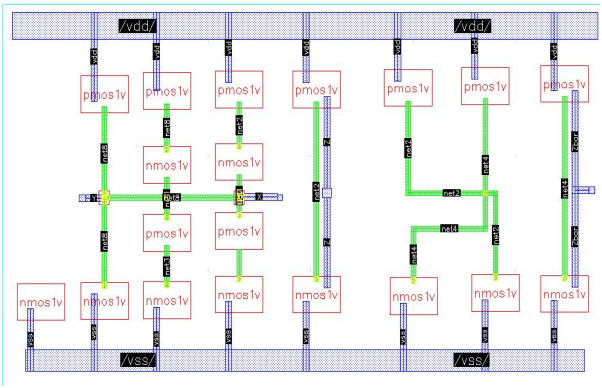


**Figure 9. Layout for the instrumentation amplifier**

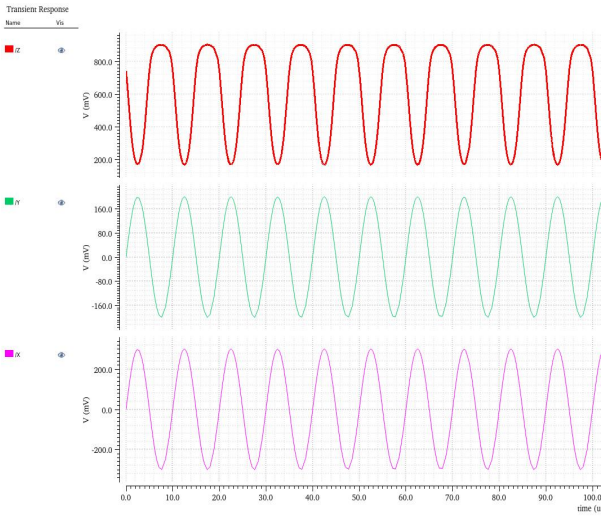

**Figure. 10 shows the gain output for the proposed instrumentation amplifier**

The characteristics of the instrumentation amplifier can be proved by using CCCII. The performance of the proposed design is also verified using DC analysis, and its characteristics are shown in Figure. 8. The layout diagram of CCCII model is displayed in Figure. 9. The layout of the CCCII occupies 15.39 mm chip area. Cadence layout design tools have been used for producing the CCCII layout. Figure. 10 shows the gain characteristics for the proposed instrumentation amplifier. In this proposed instrumentation amplifier, have two passive components(resistors) One resistor will be stable the other is variable from 10 to 50kΩ. By varying the passive components, the gain of the amplifier can be varied and also a high-frequency signal is produced while the bias current is kept unchanged.

In this instrumentation amplifier development, various configurations have been explored, each offering unique insights and characteristics. Reference [11] delves into the analysis of an instrumentation amplifier crafted using a 1.5 µm CMOS process from TSMC. This configuration operates with a supply voltage of ±2.5V and employs three Operational Amplifiers (OPA). While power consumption specifications aren't provided, the focus lies on the circuit's architecture and performance. Moving forward, Reference [18] contributes findings from a configuration utilizing a 0.25 µm CMOS process from TSMC. This setup operates with a supply voltage of ±1.5V and consumes 1.74 mW. Here, a single Differential Voltage Current Conveyor (DVCC) is employed, emphasizing efficiency and power optimization.

TABLE. 2 COMPARISON BETWEEN THE PROPOSED INSTRUMENTATION AMPLIFIER AND OTHERS PRESENTED IN THE LITERATURE

| Reference | [11] | [18] | [19] | [20] | [22] | **Proposed design** |
|---|---|---|---|---|---|---|
| Technology CMOS | 1.5 µm TSMC | 0.25 µm TSMC | 0.35 µm TSMC | 0.35 µm TSMC | 0.18 µm TSMC | **0.045 µm TSMC** |
| Supply voltage(V) | ±2.5 | ±1.5 | ±0.75 | ±3.3 | ±0.18 | **±1** |
| Power dissipation (mW) | --- | 1.74 | 3.5 | 0.159 | 0.492 | **0.137** |
| Number of active devices | 3 OPA | 1 DVCC | 3 CCCII | 2 CCCII | 1 DDCC | **1 CCCII** |

In Reference [19], attention shifts to a 0.35 µm CMOS process from TSMC. With a supply voltage of ±0.75V, this configuration consumes 3.5 mW. The circuit design involves three Current Controlled Conveyor Transconductance Amplifiers (CI), highlighting versatility and functionality. Similarly, Reference [20] explores another 0.35 µm CMOS process from TSMC, albeit with a higher supply voltage of ±3.3V. Remarkably, despite the elevated voltage, power consumption is reduced to 0.159

mW. This setup employs two Current amplifiers, indicating a balanced approach to performance and efficiency. Lastly, Reference [22] presents insights from a configuration utilizing a 0.18 µm CMOS process from TSMC. Operating with a supply voltage of ±0.18V, this setup consumes 0.492 mW. Notably, the proposed instrumentation amplifier is advantageous in many signal processing and biomedical applications and showcasing innovative design choices for enhanced performance in low-power applications.

## 6. CONCLUSIONS

The high CMRR voltage mode instrumentation amplifier using CCCII realized demonstrates promising performance characteristics. With a maximum gain of 9.03 dB, it offers significant signal amplification capabilities. The delay of 0.125mW indicates efficient signal propagation through the amplifier circuit. Furthermore, the average power consumption of 0.137mW showcases reasonable energy efficiency. The completion of schematic, symbol, and layout designs ensures a comprehensive understanding of the amplifier's architecture. Additionally, thorough analyses including DC power, transient behavior, and frequency response provide valuable insights into its operational characteristics. Graphical representations depicting frequency versus output resistance and frequency versus gain further enhance our understanding of the amplifier's behavior across different operating conditions. Overall, the amplifier design exhibits promising performance metrics and is well-equipped for various signal-processing applications

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